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TITLE

METHOD FOR FORMING A CONTACT OPENING

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a semiconductor process. In particular, the present invention relates to a method of using an image resist acting as a sacrificial layer for an inter-level dielectrics (ILD), and forming a contact opening in inter-level dielectrics (ILD) without etching.

Description of the Related Art

As ICs become more compact, semiconductor designs have reduced device dimensions. For example, the 64M DRAM process has shifted from 0.35μm to 0.3μm or less, and the 128M and 256M DRAM process to less than 0.2μm.

In the contact process of the array area of a memory unit, the transistor arranges with high density, so a self-aligned contact (SAC) process is typically employed to enhance precision and accuracy. First, the (boro-phosphosilicate glass (BPSG), tetracthoxysilane (TEOS) stacked layers, and the silicon oxide materials, are used to as an inter-level dielectrics (ILD, the insulator layer) covering the transistors, then a SAC bit line contact (CB holes) is formed in the insulator layer using an etching process, the polysilicon material is then filled into the bit line contact to serve as a bit line contact plug. Subsequently, a contact holes process is carried out in the

array area which a gate electrode contact (CG holes) and a junction contact (CS contact) are formed in the above insulator layer. Next, the bit line conductive wire M0 is etched to define the contact location of the bit line contact plug.

When the ILD is etched, the BPSG/TEOS insulator layer is etched through to expose junction area, exposing the silicon substrate to potential damaged, which results in a serious sub-threshold Voltage (sub-Vt) problem, impacting the memory ability of the capacitor in the array area. Additionally, when the ILD is etched, the spacers on the sidewall of the gate electrodes (word line) are easily damaged, resulting in short circuits between word line and bit line. Moreover, when a semiconductor design has reduced device dimensions, the width between the gate electrodes is reduced, impeding the etching process, and resulting in open circuits.

FIGS. 1~2 show the conventional self-aligned contact fabrication resulting in bit line open circuits or word line/bit line short circuits.

Subsequently, in FIG. 1, the pad silicon nitride layer 28, the BPSG layer 30, and the TEOS 32 stacked insulator layer are formed on the silicon substrate 10 with the transistor structure, wherein the pad silicon nitride layer 28 is employed to prevent the B^+/P^+ of the BPSG layer 30 diffusing to the silicon substrate 10 when a thermal process is performed, impacting the device characteristics. The transistor includes source 12, drain 14 and gate structure 20, the gate structure 20 includes gate oxide layer 21, polysilicon layer 22, tungsten silicon layer 23, silicon

nitride layer 24 and silicon nitride spacer 25, on the sidewall of the gate structure 20, wherein the gate electrode consists of the polysilicon layer 22 and the tungsten silicon layer 23. Next, a resist layer 40 is formed on the TEOS layer 32, with a contact opening pattern, then, using the resist layer 40 as a mask, the BPSG layer 30/TEOS layer 32 is etched to form a contact opening 34. Since the contact opening 34 widths of the exposed drain area 14 between the gate electrodes are less than 0.030um when the line width is minimized to about 0.09μm, and, the BPSG layer 30/TEOS layer 32 stacked insulator layer is very thick, the ILD is more difficult to etch when closer to drain area 14, and once the etching reaction is complete, incomplete or unetched insulator residue 30' remains in the bottom of the contact opening 34, preventing exposure of the drain area 14. When the insulator residue 30' is not a conductor, the subsequently filled conductive material cannot be electrically connected, resulting in the described bit line contact open circuits.

In order to prevent open circuits, in FIG. 2, a conventional method uses overetching to etch the insulator residue 30' and the pad silicon nitride layer 28, however, the etching selectivity of the silicon oxide material to the silicon nitride spacer is only around 10~15, and the silicon nitride layer 24 and the silicon nitride spacer 25 are easily removed, exposing the tungsten silicon 23 and polysilicon 22 of the gate electrodes, resulting in word-line/bit-line short circuits.

Additionally, BPSG possess excellent gap filling characteristics even if the line width is reduced to 0.09 or

0.07um; however, the width between the gate electrodes is minimized when the line width dimension is reduced, such that the gap between the gate electrodes is difficult to fill even with BPSG material, resulting in voids and leading to short circuits between the adjacent contacts of the individual bit lines. Different from FIG. 1 and 2, FIG. 3 shows that the two drains 14 are a portion of the transistor of the individual bit line. After etching the BPSG 30 and TEOS 32 stacked insulator layer to form a contact opening 34 using resist layer 40 as a mask, the resist layer 40 is then removed. Next, the contact opening 34 is filled with conductive material to form bit line contact plug 38. Once the contact opening 34 forms void 36, the conductive material is also filled into the void 36, resulting in short circuits between contact plugs 38 of adjacent bit lines.

SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to provide a method of forming a contact opening, and preventing the silicon substrate from damage during, for example, bit line contact etching.

Another object of the invention is to provide a method of forming a contact opening, and preventing the contact from open circuits due to narrow width between the gate electrodes.

Another object of the invention is to provide a method of forming a contact opening, and preventing word line/bit line from short circuits.

Another object of the invention is to provide a bit line contact process, and preventing contact plugs from

short circuits due to the voids in the inter layer dielectric (ILD).

In order to achieve the above objects, the invention provides a method of forming a contact opening, comprising providing a substrate with transistors protected by a silicon-containing insulator layer, then, covering a non-silicon-containing resist layer on the substrate, with a level surface, next, covering a silicon-containing thin resist layer on the non-silicon-containing resist layer to form a stacked resist layer, with a level surface, patterning the stacked resist layer to form a resist stacked layer with a contact plug pattern overlying the doping areas, next, forming an insulator layer on the resist unmasked area using a selective deposition process, removing the stacked resist layer to expose the doping area, and forming a contact opening.

DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference is made to a detailed description to act as read of conjunction with the accompanying drawings, in which:

FIG. 1 is a cross section of the bit line open circuits in the conventional bit line contact process.

FIG. 2 is a cross section of the word-line/bit-line short circuits in the conventional bit line contact process.

FIG 3 is a cross section of the short circuits between contacts of the adjacent bit line in the conventional bit line contact process.

FIG.4A~4F are cross sections of the method of forming the bit line contact opening according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In this specification, "overlying the substrate", "above the layer", or "on the film" denote a relative positional relationship with respect to the surface of the base layer, regardless of the existence of intermediate layers. Accordingly, these expressions may indicate not only the direct contact of layers, but also, a non-contact state between one or more laminated layers.

In FIG. 4A, a semiconductor substrate 100, such as a single crystal substrate, is provided with a transistor 102 thereon, the transistor consists of source 142, drain 144, gate insulator layer 150, polysilicon layer 152, metal silicide layer 154 and mask layer 156. A gate electrode constituted by polysilicon layer 152 and metal silicide layer 154 and covered by an insulating material, capped by a silicon nitride layer as a mask layer 156, with a silicon nitride spacer 158 on the sidewall. That is, a transistor 102 constitutes a gate electrode covered by an insulator material; a drain 142 and a source 144 are the doping area, with a spacer 103 between the adjacent transistors 102.

In present invention, since the inter layer dielectric (ILD) uses a non-boron/phosphorous silicon oxide material instead, the spacer 103 on the exposed semiconductor substrate 100 is not necessarily protected by an additional pad silicon nitride layer, such that the boron/phosphorous

of the BPSG is preventing from diffusing to the substrate, thus eliminating a step of the deposition process.

In FIG. 4B, an non-silicon-contained resist layer 104, such as model number NFL1400, produced by JSR Company, is coated on the substrate 100 of the formed transistor 102, with a thickness of about 4000~8000Å and a level surface, then, a silicon-containing thin image resist layer 106 is coated on the non-silicon-containing resist layer 104, with a thickness of about 500~4000Å (optimal is 800~2000Å) and a level surface to obtain an optimal resolution after deep ultraviolet light (DUV) exposure and a development process.

In FIG. 4C, after deep ultraviolet light (DUV) exposure, with a light source such as ArF 193nm or KrF 248nm, the pattern of the bit line contact is defined on the silicon-containing resist layer 106. Subsequently, using the patterned image resist layer 106 as a mask, the non-silicon-containing resist layer 104 thereunder unmasked by image resist layer 106 is removed using an etching process, such as SO_2/O_2 etching, exposing the non-bit-line-contact area with a silicon-containing surface, such as a silicon substrate surface.

In FIG. 4D, a silicon oxide layer is deposited on the silicon substrate surface using liquid phase oxide deposition (LPOD), layer by layer, the gaps between the resist stacked layer 104/106 are filled to form a silicon oxide layer 108, with a thickness of about 5000~8000Å depending on the real depth of the M0 bit line.

The process of the liquid phase oxide deposition (LPOD), for example, is to immerse the surface of the substrate in hexafluorosilicic acid (H_2SiF_6) solution, and

adding boric acid (H_3BO_3), the reaction formulas are as follows:

$$H_2SiF_6 + 2\ H2O \quad SiO_2 + 6\ HF$$

$$H_3BO_3 + 4\ HF \quad BF_4^- + H_3O^+ + 2\ H_2O$$

Another method is to immerse the surface of the substrate in H_2SiF_6 and NH_3 solutions, the reaction formulas are as follows:

$$H_2SiF_6 + 2\ NH_3 \quad (NH_4)_2SiF_6$$

$$(NH_4)_2SiF_6 + 4\ NH_3 + 2\ H_2O \quad SiO_{2(s)} + 6\ NH_4F$$

The above mentioned liquid phase oxide deposition (LPOD) processes are exemplary and are not restricted thereto. Other liquid phase oxide deposition (LPOD) processes can be used instead.

Next, in FIG. 4E, the resist stacked layers 104 and 106 are removed using conventional O_3 plasma etching to expose the doping area 144 of the bit line contact, and then cleaned by a H_2SO_4/H_2O_2/DHF mixed acid solution.

Subsequent to the above process steps, a contact opening 110 for bit line contact is formed in silicon oxide layer 108. Next, in FIG. 4F, a TiN and a Tungsten (W) or polysilicon conductive material are filled sequentially into the contact opening 110, then, the unnecessary portion of the conductive material is removed using chemical mechanical polishing (CMP) to form a bit line contact plug 120 in the contact opening 110.

The invention of forming a contact opening uses a lithography process to first mask the area of the bit line contact, then forms the silicon oxide layer on the surface of the silicon oxide and silicon using selective deposition, eliminating an etching process step and preventing damage to

the silicon from an etching process, such as overetching which resulting in word line/bit line short circuits; or incomplete etching which results in bit line open circuits; as well as preventing void formation in the ILD.

Moreover, the invention uses ILD without boron/phosphorous, therefore, the pad silicon nitride layer need not be protected from boron/phosphorous diffusion, thus eliminating a process step of the pad silicon nitride deposition.

Although the present invention has been particularly shown and described above with reference to the preferred embodiment, it is anticipated that alterations and modifications thereof will no doubt become apparent to those skilled in the art. It is therefore intended that the following claims be interpreted as covering all such alteration and modifications as fall within the true spirit and scope of the present invention.